SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

EXTERNAL DMA MODE I/O DATA TRANSFER SYNCHRONIZED BY TIMER

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INTRODUCTION

ST9 provides a powerful features allowing DMA transfers between I/O port and Register file or memory spaces (Program/Data memory). Furthermore DMA operations on I/O port can be done under handshake control and with swap mode capability.

The DMA transfer between external I/O port and memory fields (Register file, Program memory, Data memory) is possible with the help of the two Timer DMA channels (COMPARE 0 and CAPTURE 0) and only one byte transfer is performed at any request (instead of two bytes when DMA takes place between Register file/Memory spaces and Compare/Capture register).

Three Timer DMA external modes on I/O port are possible:

- COMPARE 0 channel external mode allowing only output data transfer.
- CAPTURE 0 channel external mode allowing bidirectional data transfer. (The direction of the data transfer is set by a bit in the I/O port control register.)
- CAPTURE 0 channel external mode synchronized by a COMPARE 0 event.

For these three modes, the synchronization is accomplished by an internal synchronization signal or by a Timer On-Chip Event signal (ie. COMPARE 0 or OVERFLOW/UNDERFLOW event).

To enable such transfers, user has to program:

- the Timer in CAPTURE or COMPARE or both DMA mode
- two Timer control bits (DCTS and DCTD) in Interrupt/DMA Control Register IDCR
- the Timer On-Chip Event and the handshake /DMA control register of the relevant I/O port.

Please refer to the note for a better understanding of the internal connection between ST9 TIMER and I/O port.

Note: On **ST9030**, the On-Chip Event of **TIMER 1** controls the handshake function with I/O Port 5, the On-Chip Event of Timer 0 is connected to the internal trigger of the A/D converter.

On **ST9020**, the On-Chip Event of **TIMER 0** controls the handshake function with I/O Port 5.

On **ST9050**, the On-Chip Event of **TIMER 0** controls the handshake function with I/O Port 4, the On-Chip Event output of Timer 1 controls the handshake function with I/O Port 5, the On-Chip Event of Timer 3 is connected to the internal trigger of the A/D Converter.

Furthermore, the Timer's output signals T0OUTA and T1OUTA may be software connected respectively to the same Timer's input signals T0INA and T1INA.

TIMER DMA EXTERNAL MODE CONTROL BITS

To program the Timer and I/O port in DMA external mode, user has to set:

- two control bits in Timer Interrupt/DMA Control Register (IDCR)
- two bits in the I/O Connection Register (IOCR)
- the Timer On-Chip Event and four control bit in the handshake/DMA Control Register (HDCTL) of the relevant I/O port.

TIMER CONTROL BITS

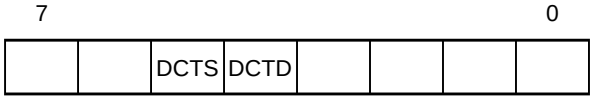
DMA transfer configuration bits

Two bits located in the Timer Interrupt/DMA Control Register (IDCR) select the source or the destination of the DMA transfer.

IDCR R243 (F3h) or R247 (F7h)

Interrupt/DMA Control Register

Page 9 or 13 Read/Write
Reset value: 10100111b (A7h)



b5 = **DCTS:** DMA Capture Transfer Source. This bit selects the source of the DMA operation related to the channel associated to CAPTURE 0.

DCTS = "0": The DMA transfer source is the Capture 0 register

DCTS = "1": The DMA transfer source is the I/O port

b4 = **DCTD**: DMA Compare Transfer Destination. This bit selects the destination of the DMA operation related to the channel associated to the COMPARE 0.

DCTD = "0": The DMA transfer destination is the COMPARE 0 register

DCTD = "1": The DMA transfer destination is the I/O port

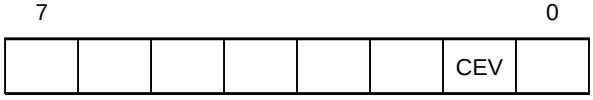
OEV, CEV: Timer On-Chip Event

These two bits, located in the output control registers (OACR and OBCR), select the event source strobing the data transfer on I/O port.

OACR R252 (FCh)

Output A Control Register

Page 8 (10, 12, 14) Read/Write
Reset value: xxxxxx0xb



b1 = **CEV** : On-Chip Event on COMPARE 0

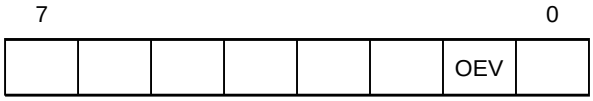
CEV = "1": On-Chip Event on successful COMPARE 0 event

TIMER CONTROL BITS (Continued)

OBCR R253 (FDh)

Output B Control Register

Page 8 (10,12,14) Read/Write
Reset value: xxxxxx0xb



b1 = **OEV :** On-Chip Event on OVERFLOW/UNDERFLOW

OEV = "1": On-Chip Event on OVERFLOW/UNDERFLOW event

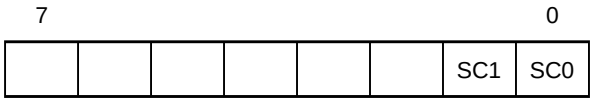
SC1, SC2: Timer I/O Connection bits

These two bits, located in the I/O Connection Register (IOCR), select (or not) an on-chip connection between input A and output B of the same Timer.

IOCR R248 (F8h)

I/O Connection Register

Page 9 or 13 Read/Write
Reset value: xxxxxx00b



b1 = **SC1**: Select connection odd.
Selects if connection between TxOUTA and TxINA for odd timer (x = 1 or 3) is done on-chip or externally.

SC1 = "0" TxOUTA and TxINA unconnected

SC1 = "1" TxOUTA and TxINA connected

b0 = **SC0**: Select connection even.
Selects if connection between TxOUTA and TxINA for even timer (x = 0 or 2) is done on-chip or externally.

SC0 = "0" TxOUTA and TxINA unconnected

SC0 = "1" TxOUTA and TxINA connected

I/O PORT CONTROL BITS

Apart from the three bits used for handshake programing, four bits located in the Handshake/DMA Control Register (HDCTL) of the relevant I/O port are used to control the DMA mode.

HDCTL

Handshake/DMA Control Register

R255 (FFh) Page 2 Handshake on Port 3

R251 (FBh) Page 2 Handshake on Port 2

R247 (F7h) Page 3 Handshake on Port 5

R243 (F3h) Page 3 Handshake on Port 4

Read/Write
Reset value: FFh

7							0
			DEN	DD	DST	DCH	1

b4 **= DEN:** DMA enable bit

DEN = 0: enable the DMA mode on I/O port

DEN = 1: disable the DMA mode on I/O port

b3 **= DD:** DMA DATA Direction bit

DD sets the DMA direction for the DMA transfer on CAPTURE 0 channel

DD = 0: output data on I/O port

DD = 1: input data from I/O port

b2 **= DST**: DMA strobe bit

DST bit selects I/O port strobe from internal synchronisation signal or from Timer On-Chip Event.

DST = 0: Internal synchronization strobe

DST = 1: Timer On-Chip Event strobe

b1 **= DCH**: DMA channel mode

DCH bit selects the DMA channel from CAPTURE 0 or COMPARE 0

DCH = 0: CAPTURE 0 DMA channel

DCH = 1: COMPARE 0 DMA channel

TIMER DMA TRANSFER ON COMPARE 0 CHANNEL

Principle

This mode, enabled when DCTD (DMA Compare Transaction Destination) bit is equal to “1”, allows output transfer from Register File/memory to an I/O port at fixed period. In this mode, DMA direction transfer always outputs Data on I/O port. A one byte output DMA transfer is done on a COMPARE 0 request caused by a COMPARE 0 event or a software COMPARE 0 request (by writing “1” in the CM0 bit in Timer Flag Register).

The data strobe is made by an internal synchronization signal on COMPARE 0 event or by a Timer OVERFLOW/UNDERFLOW On-Chip Event.

Figure 1 shows the principle of COMPARE 0 channel external mode.

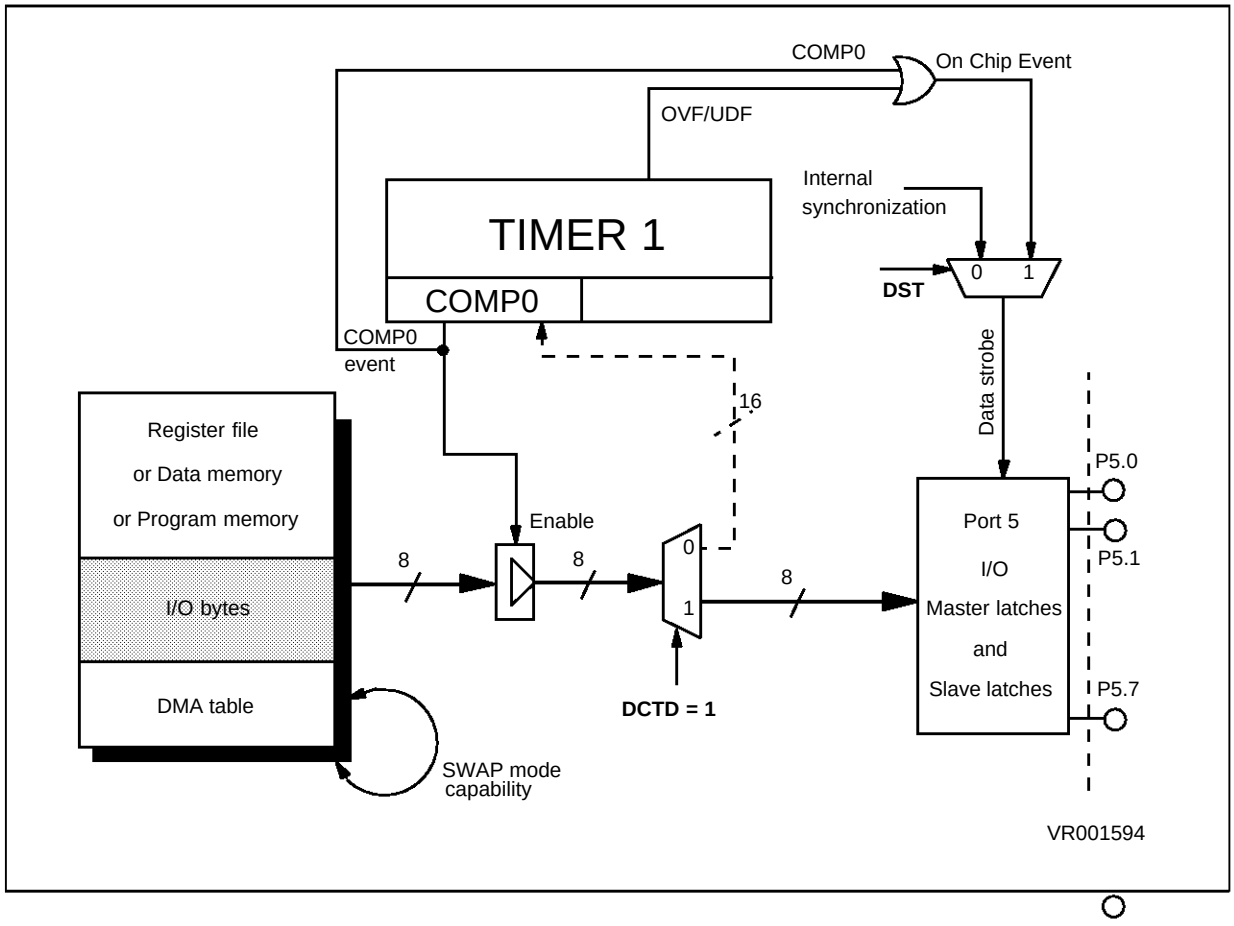
Programmation

To program Timer in DMA transfer mode on COMPARE 0 channel, user has to:

- program the Timer in COMPARE 0 channel DMA mode
- select the I/O port as destination for DMA transfer by setting the DCTD bit in IDCR
- select the data strobe mode by programming the on chip event (internal data synchronization, Timer on chip event data strobe)
- Program the relevant I/O port by clearing the DEN bit to enable DMA mode, choose the data strobe mode (DST bit) and select the COMPARE 0 DMA channel (DCH bit).
- start DMA transfer by enabling the Timer count.

Such a programmation is shown in appendix A.

Figure 1. Timer DMA Transfer on COMPARE 0 Channel Principle



TIMER DMA TRANSFER ON CAPTURE 0 CHANNEL

Principle

This mode, enabled when DCTS (DMA Capture Transaction Source) bit is equal to "1", allows bidirectional transfer from register file/memory to/from I/O port. In this mode, the DMA transfer direction is set by the DMA direction bit in HDCTL register. The DMA transfer is done on a CAPTURE 0 request caused by an external CAPTURE event or by a software CAPTURE 0 request (by writing "1" in the CP0 bit in Timer Flag Register). The data strobe is either an internal synchronization signal on CAPTURE 0 event or a Timer COMPARE 0 or OVERFLOW/UNDERFLOW On-Chip Event.

Figure 2 shows the principle of CAPTURE 0 channel external mode

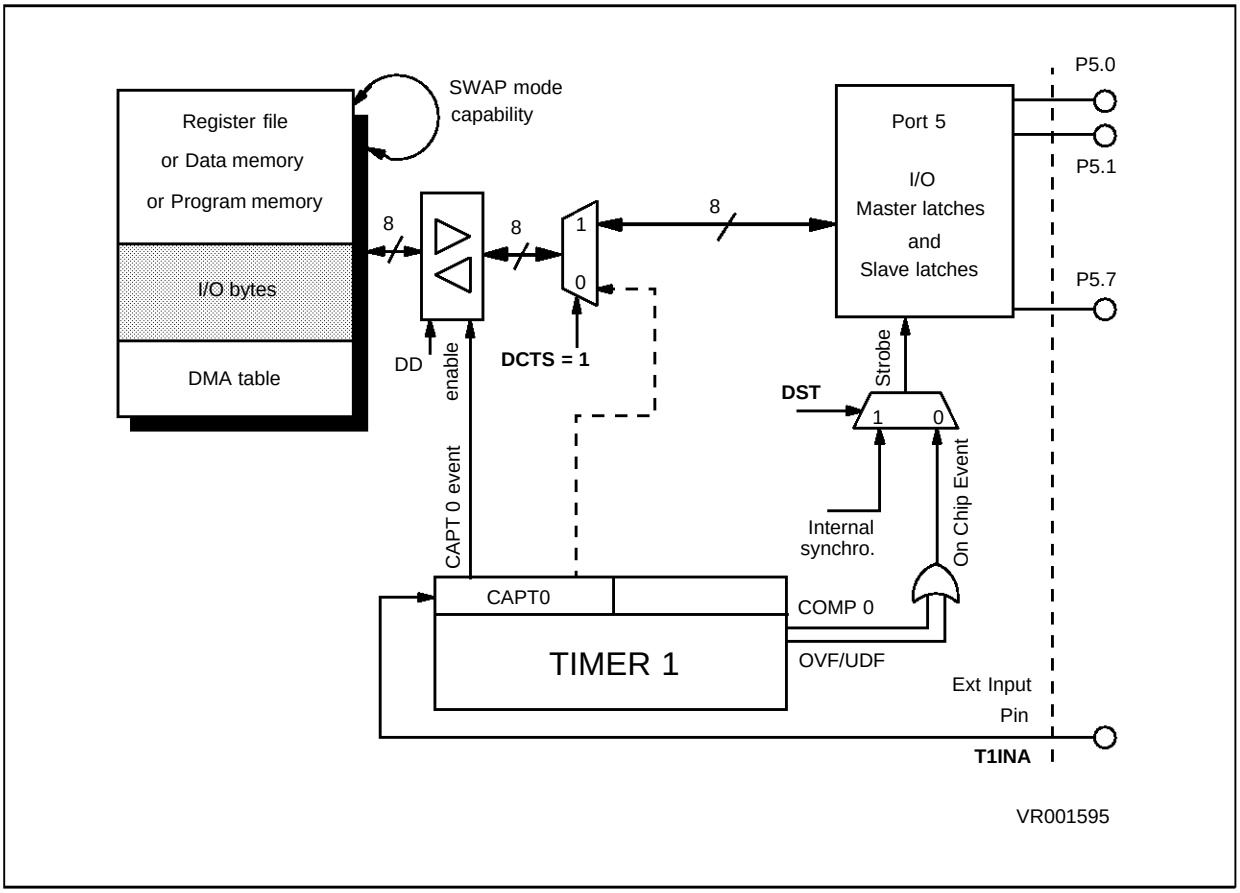
Programmation

To program Timer in DMA transfer mode on CAPTURE 0 channel, user has to:

- program the Timer in CAPTURE 0 channel DMA mode
- select the I/O port as destination for DMA transfer by setting the DCTS bit (in IDCR)
- select the data strobe mode by programming the On-Chip Event (internal data synchronization or Timer On-Chip Event strobe)
- program the relevant I/O port by clearing the DEN bit to enable DMA mode, set the DMA transfer direction (DD bit), choose the Data strobe mode (DST bit) and select the CAPTURE 0 DMA channel (DCH bit).
- start DMA transfer by enabling the Timer count.

Such a programmation is shown in appendix B.

Figure 2. Timer DMA Transfer on CAPTURE 0 Channel Principle



DMA SEQUENCER: CAPTURE 0 CHANNEL SYNCHRONIZED BY COMPARE 0 CHANNEL

Principle

This mode, using two DMA channels, allows bidirectional DMA Data transfer between I/O port and register file/memory spaces at variable throughput. This Timer DMA transfer mode uses the CAPTURE 0 channel to provide bidirectional transfer on each CAPTURE 0 event. This Capture 0 event is triggered by the COMPARE 0 channel by an output toggle on COMPARE 0 internally fed back to CAPTURE 0. Like in the previous mode, the data strobe is made by an internal synchronization signal on CAPTURE event or by a Timer COMPARE 0 or OVERFLOW/UNDERFLOW On-Chip Event.

Figure 3 shows the principle of CAPTURE 0 synchronized by COMPARE 0 event.

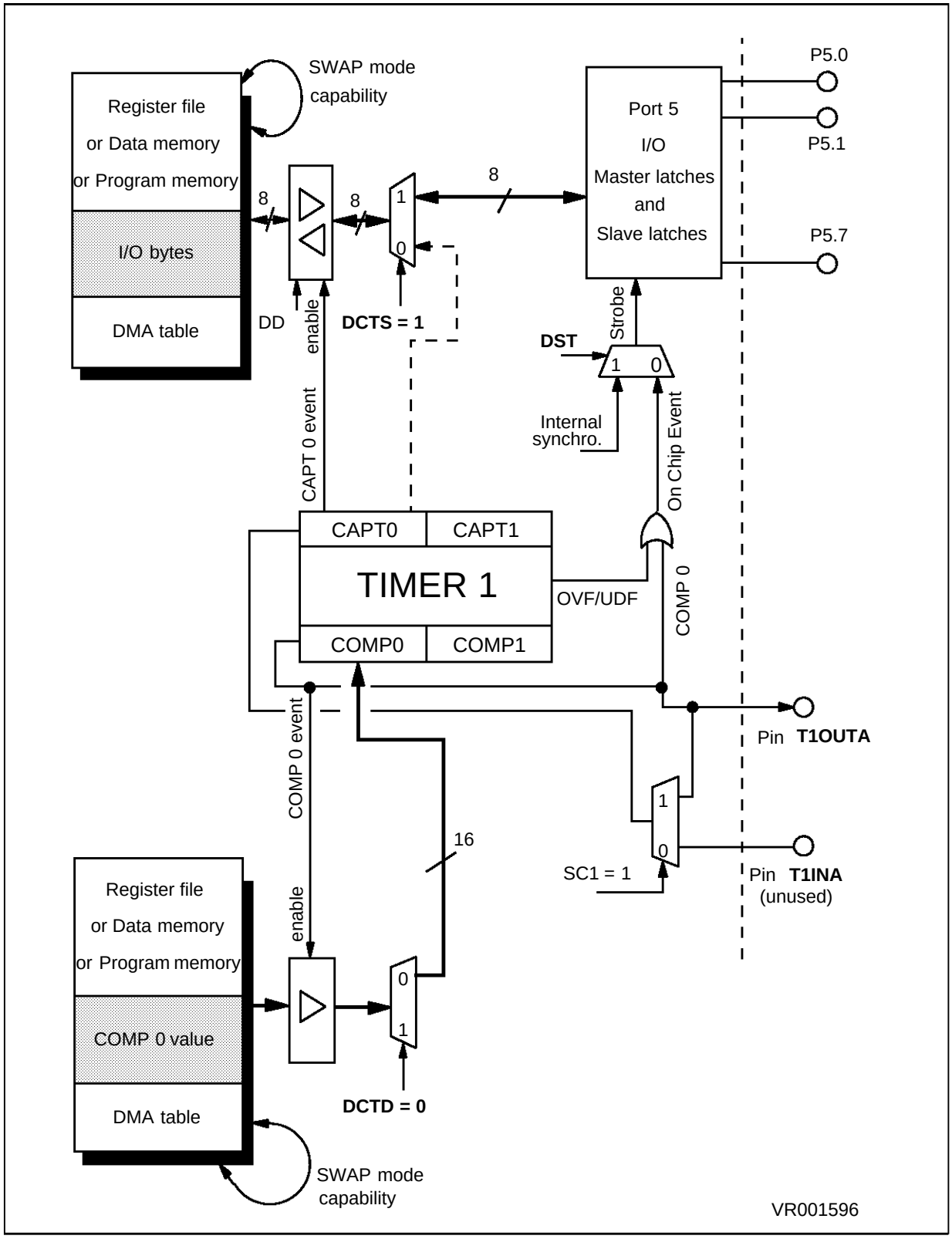
Programmation

To program Timer in DMA transfer on CAPTURE 0 synchronized by COMPARE channel, the user has to:

- program the timer in CAPTURE 0 channel DMA external mode and in COMPARE 0 DMA mode with an output toggle action on T1OUTA
- select I/O port as destination for DMA transfer by setting the DCTS bit in IDCR
- select the data strobe mode by programming the On-Chip Event (internal synchronization or Timer On-Chip Event strobe)
- program the relevant I/O port by clearing the DEN bit to enable DMA mode, set the DMA transfer destination (DD bit), choose the Data strobe mode (DST bit) and select the Capture 0 DMA channel (DCH bit)
- internally connect the timer 1 output A (T1OUTA) on the timer input A (T1INA) by setting SC1 bit in I/O Control Register (IOCR)
- start the DMA transfer by enabling the Timer count.

Such a programmation is shown in appendix C.

Figure 3. Timer DMA Transfer on CAPTURE 0 Channel Principle

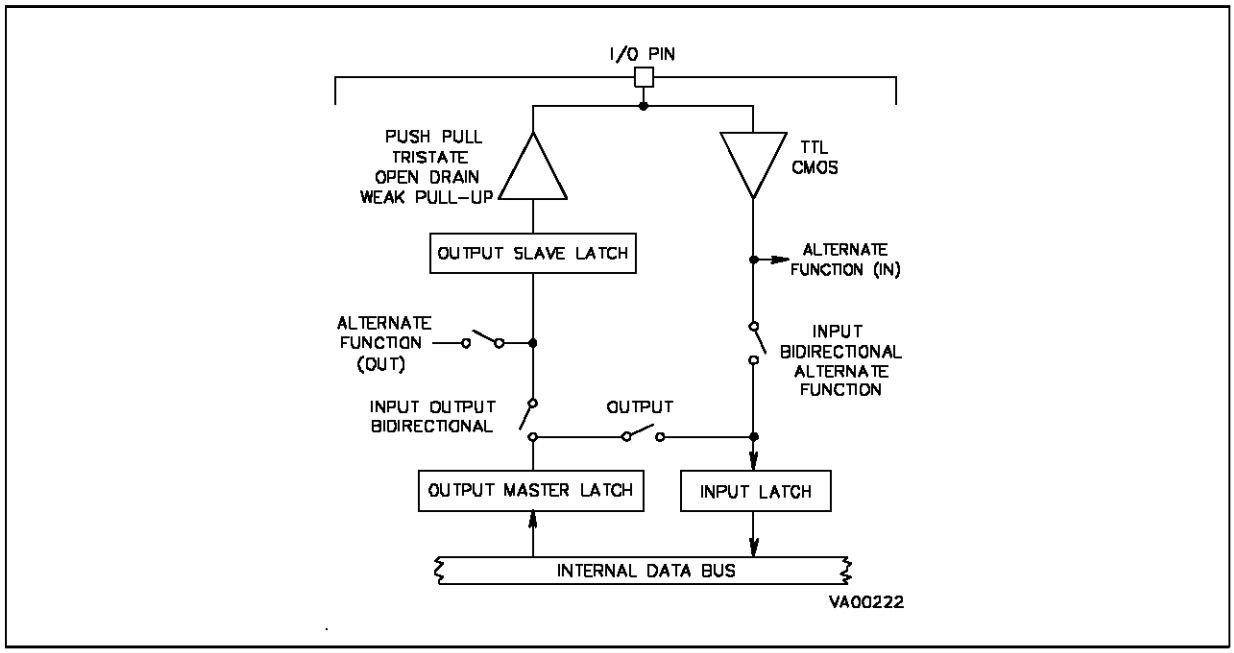


DATA OUTPUT SYNCHRONIZATION ON I/O PORT

Data Output During an Instruction Execution

The basic structure of an I/O pin shows that an I/O port is driven by an output slave latch and by an output master latch as shown in the following Figure.

Figure 4. Basic Structure of an I/O Port Pin

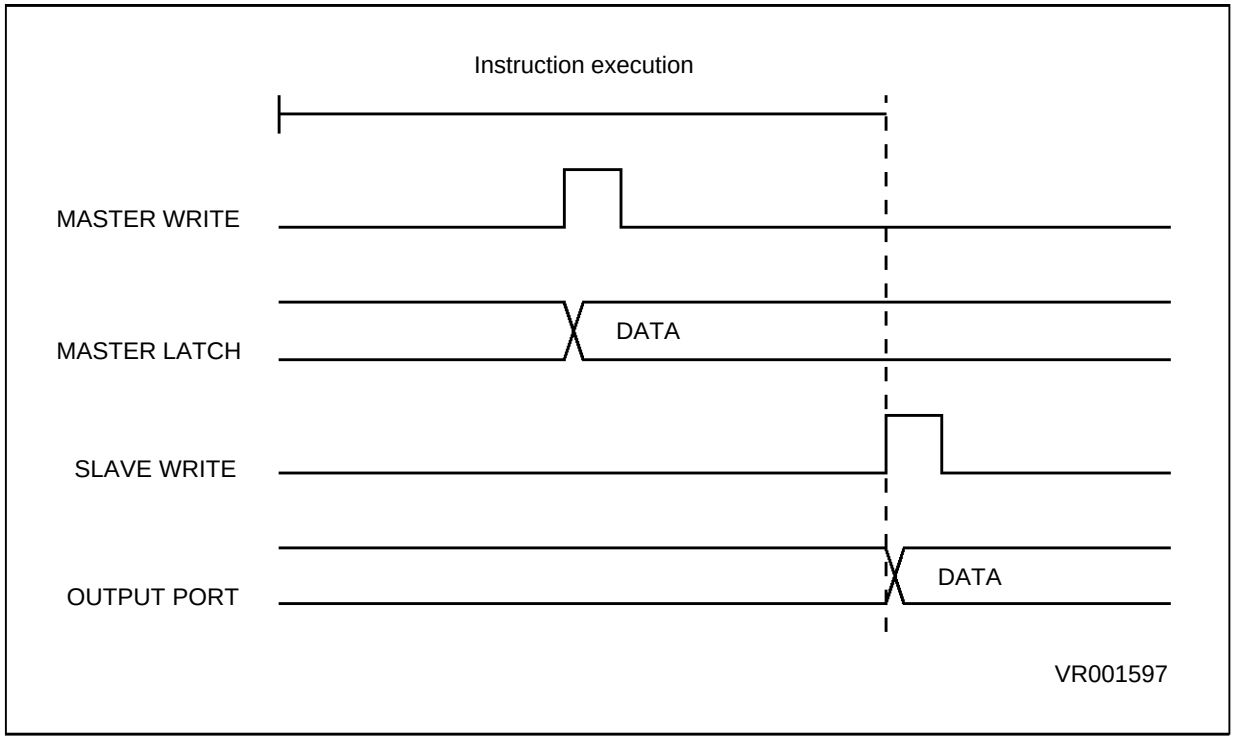


DATA OUTPUT SYNCHRONIZATION ON I/O PORT (Continued)

The data present on the internal data bus is copied in the output master latch during the execution of each instruction. The data stored into the output master latch is copied into the output slave latch (driving the I/O pin) at the end of each instruction. In input Mode data present on the I/O pin is sampled into the input data latch at the beginning of the execution of each instruction.

Figure 5 shows the timing of such a transfer.

Figure 5. Data Output During an Instruction Execution



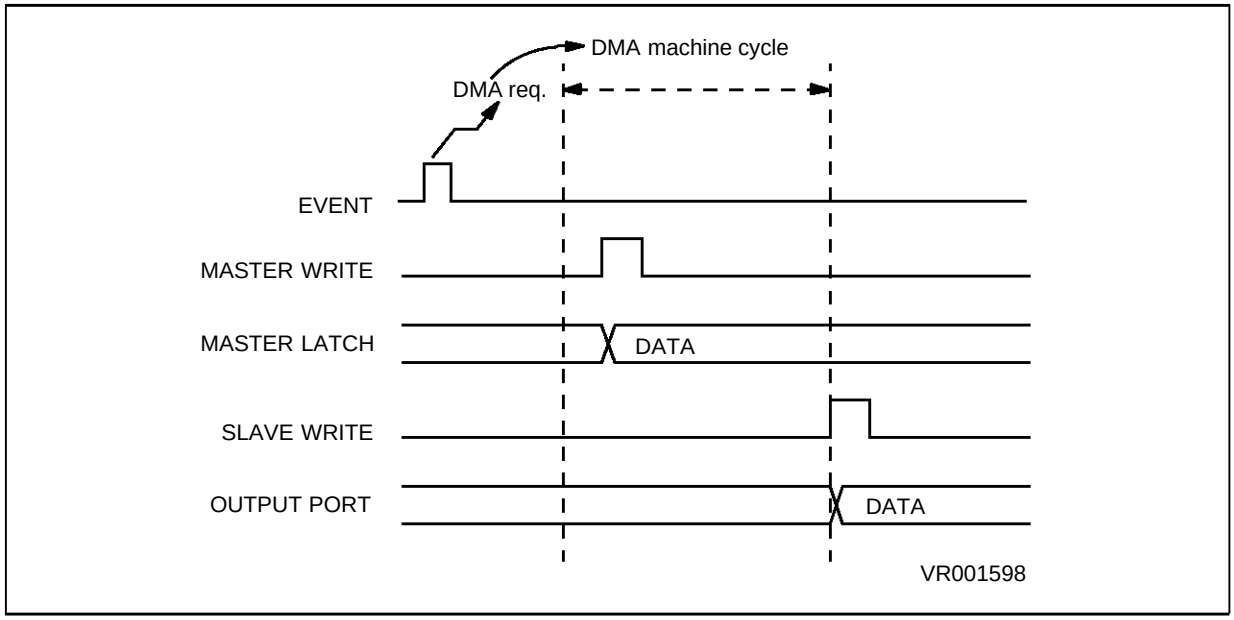
DATA OUTPUT SYNCHRONIZATION ON I/O PORT (Continued)

Data Output when Using Regular DMA Mode

In regular DMA mode, an internal synchronization signal, (depending on the DMA channel used: CAPTURE 0 channel or COMPARE 0 channel), is used to strobe the data on I/O port. In this mode, the data present on the internal data bus is copied into the output master latch during the DMA machine cycle. The data stored into the output master latch is copied into the output slave latch driving I/O pin at the end of the DMA machine cycle.

Figure 6 shows the timing of such a transfer.

Figure 6. Data Output with Regular DMA Mode



DATA OUTPUT SYNCHRONIZATION ON I/O PORT (Continued)

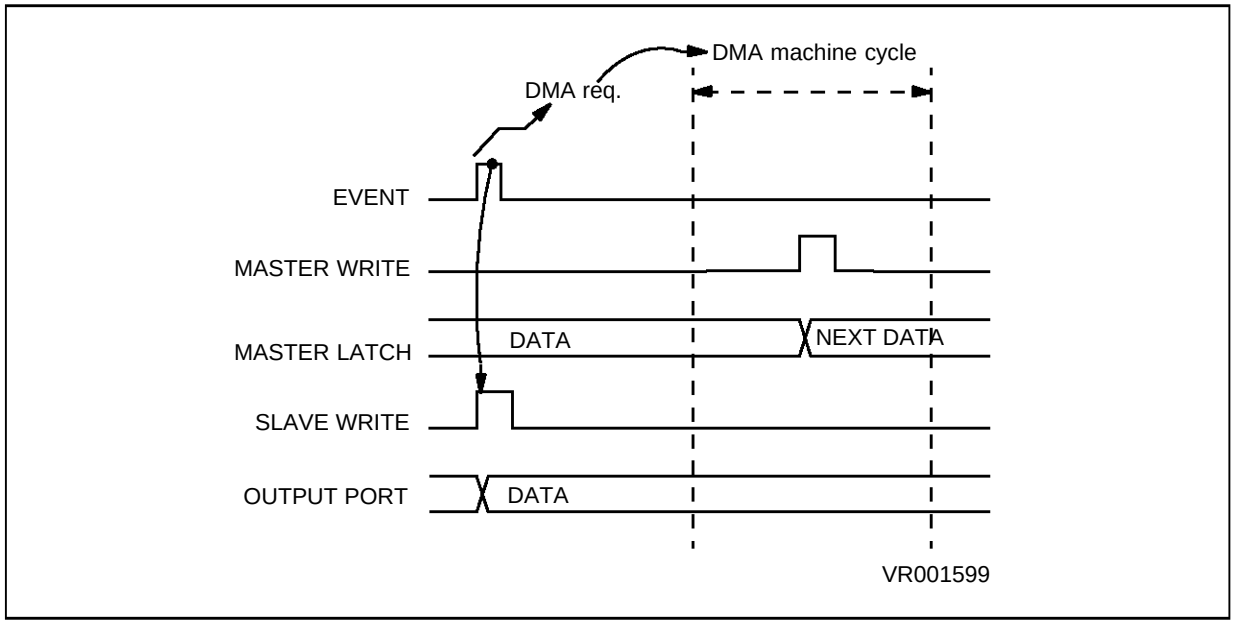
Data Output with DMA "On-Chip Event" Mode

In this mode, the data synchronization on I/O port is done by the Timer On-Chip Event signal (COMPARE 0 On-Chip Event, OVERFLOW/UNDERFLOW On-Chip Event).

The data present in the output master latch is copied into the output slave latch driving the I/O pin when the On-Chip Event occurs. The data present on the internal data bus is copied into the output master latch during the following DMA machine cycle.

Figure 7 shows the timing of such a transfer.

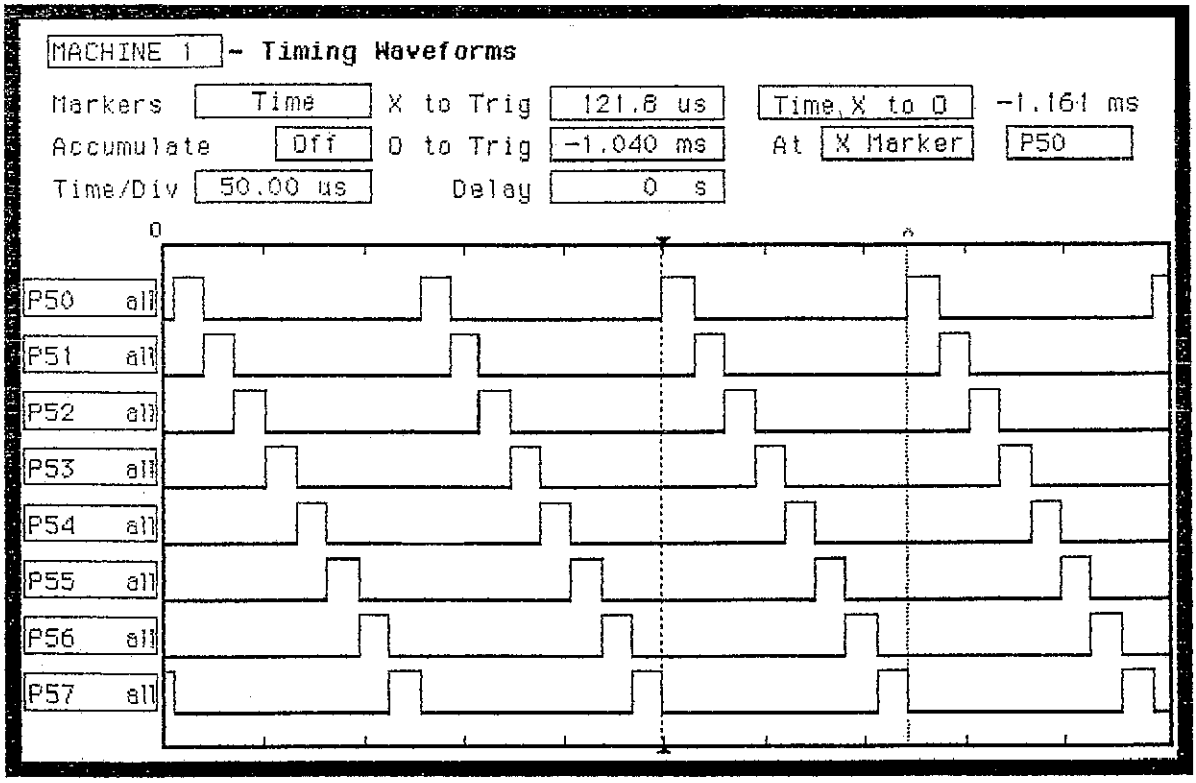
Figure 7. Data Output with DMA "On-Chip Event" mode



APPENDIX A: COMPARE 0 CHANNEL IN EXTERNAL MODE

The following examples details how to program the Timer in order to generate the waveform shown on Figure 8 .

Figure 8. Timing Waveform Example: COMPARE 0 Channel



To generate this specific waveform, the Timer is programmed to output data by a COMPARE 0 channel DMA transfer between a pattern table located in program memory (DMA_TABLE_OUT) and I/O port 5 (see TIMER_1 subroutine). A COMPARE 0 interrupt (DMA end of block interrupt) clears the successful COMPARE 0 flag and restarts the DMA transfer (see COMPARE 0 interrupt routine). I/O port 5 is configured in output in DMA mode (see INIT_IO subroutine).

APPENDIX A: COMPARE 0 CHANNEL IN EXTERNAL MODE (Continued)

```
.title  "DMA between program memory and I/O port 5 with TIMER 1 COMPARE 0 channel"

;This program is a small example of using Timer 1 DMA external mode on I/O port
;The timer is programmed in COMPARE0 DMA channel EXT mode

;***************************
;*INTERRUPT VECTOR ADDRESSES*
;***************************

CORE_IT_VECT    :=          00h             ; Core interrupts vectors
T1_IT_VECT      :=          10h             ; Timer 1 interruts vectors

CAPT_IT_VECT    =           4               ; Capture event interrupt address
COMP_IT_VECT    =           6               ; COMPARE event interrupt address
T1_LEVEL        :=          4               ; Timer 1 priority level
LG_DMA          =           8               ; length of DMA

; Define the DMA pointer register
; DMA transfer from program memory

AD_DMA_BR       =           48h             ; DMA address base register
LG_DMA_BR       =           4ch             ; DMA counter base register
CMP_AD_DMA      :=          RR#AD_DMA_BR+2  ; Compare DMA address register ptr
CMP_LG_DMA      :=          RR#LG_DMA_BR+2  ; Compare DMA counter register ptr

; Define global references

.global         RESET_START, TIMER_1, INIT_IO, COMPARE0, DMA_TABLE_OUT

;********************
;*Group number names*
;********************

BKC             :=    12
BKD             :=    13
BKE             :=    14
BKF             :=    15
BK_F            :=    BKF * 2               ; group F: page registers

;***********************
;* Start Timer 1 macro *
;***********************

.macro  START_T1
        spp     #T1D_PG                     ; select Timer 0 page
        or      T_TCR,#( cen | ccl )        ; counter enable bit, clear counter
.endm;******************
;*START of PROGRAM*
;******************

START_PROG      :=    110h                  ; start address program

;********************
;*STACK Declaration*
;********************

SSTACK          :=    ( BKE * 16 ) - 1      ; System stack address group D C
USTACK          :=    ( BKC * 16 ) - 1      ; User stack address group B
```

APPENDIX A: COMPARE 0 CHANNEL IN EXTERNAL MODE (Continued)

```
;*****************************************
;*Declaration of the interrupt vectors table*
;*****************************************
;
        .text                               ; start of program

                .org  CORE_IT_VECT          ; Core interrupt vector
                                            ; ********************
                                            ;
                .word RESET_START           ; power on interrupt vector
                .word DIV0                  ; divided by 0 subroutine trap vector
                .word TOP_LEVEL_IT          ; Top level interrupt vector

                .org  T1_IT_VECT            ; Timer 1 interrupt vectors
                                            ; ************************
                                            ;
                .org  T1_IT_VECT + 6        ; unused addres
                .word COMPARE0              ; Timer 1 compare 0 interrupt

;******************************
;* Output data table to Port 5 *
;******************************
;
                .org  100h

DMA_TABLE_OUT:  .byte 01h, 02h, 04h, 08h
                .byte 10h, 20h, 40h, 80h    ; output DMA table

;**********************
;*Start of main module*
;**********************
;
                .org  START_PROG            ; start of code

RESET_START:

        ld      MODER,#11100000b            ; CLOCK MODE REGISTER
                                            ; internal stack
                                            ; no prescaling
                                            ; external clock divided by 2

        ld      CICR,#10001111b             ; CENTRAL INTERRUPT CONTROL REGISTER
                                            ; priority level = 7
                                            ; Nested Arbitration mode
                                            ; disable interrupt
                                            ; enable counters
                                            ; At reset, Global Counter Enable bit is active.

        ld      SSPLR,#SSTACK + 1           ; load system stack pointer
        ld      USPLR,#USTACK + 1           ; load user stack pointer

        call    TIMER_1                     ; Timer 1 initialization in DMA mode

        call    INIT_IO                     ; Port 5 init. DMA mode

        START_T1                            ; Start Timer 1

        ei                                  ; enable all interrupts

;MAIN PROGRAMM

        loop    {
;               wfi
        }
```

APPENDIX A: COMPARE 0 CHANNEL IN EXTERNAL MODE (Continued)

```
;******************
;initialize TIMER 1
;******************
proc    TIMER_1 {

        srp     #BK_F                       ; select working register
        spp     #T1D_PG                     ; select timer 1 register page

        ld      t_tcr,#( ccmp0 | udc )      ; count up
                                            ; clear on compare  0

        ld      t_tmr,#0                    ; Disable output B
                                            ; Disable output A
                                            ; Internal clock
                                            ; Countinuous mode

        clr     t_icr                       ; No action on input pins
        clr     t_prsr                      ; No prescaling

        ld      t_oacr,#( ou_nop | c1_nop | c0_nop ); No action on OUTPUT0
        ld      t_obcr,#( c0_nop | c1_nop | ou_nop ); No action on OUTPUT1
        clr     t_flagr

        spp     #T1C_PG                     ; Timer 1 Control page register
        ld      t1_dcpr,#LG_DMA_BR          ; DMA counter register base address
        ld      t1_dapr,#AD_DMA_BR          ; DMA address register base address
        ld      t1_ivr,#T1_IT_VECT
        ld      t1_idcr,#( T1_LEVEL | dctd ); DMA compare transaction
        ldw     CMP_LG_DMA,#LG_DMA          ; Compare DMA counter init.
        ldw     CMP_AD_DMA,#DMA_TABLE_OUT   ; Compare DMA addres init.

        spp     #T1D_PG                     ; Timer 1 Data page
        ld      t_idmr,#( gtien | cm0i | cm0d ); Compare 0 INT and DMA

        ldw     t_reg0r,#0                  ; reg 0
        ldw     t_cmp0r,#3ch                ; 15 µs

        }
```

APPENDIX A: COMPARE 0 CHANNEL IN EXTERNAL MODE (Continued)

```
;*****************************************************************************
;                     COMPARE 0 INTERRUPT ROUTINE
;                     DMA Interrupt End of block
;*****************************************************************************

COMPARE0:

begin   [ PPR, RP0R, RP1R ] {               ; save page pointer
                                            ; save register pointer pair

        spp     #T1D_PG                     ; Timer 1 data register page
        srp     #BK_F                       ; select group F

        and     t_flagr,#~( cm0 | ocm0 )    ; reset successful compare 0
                                            ; reset overrun on compare 0

        ldw     CMP_LG_DMA,#LG_DMA
        ldw     CMP_AD_DMA,#DMA_TABLE_OUT
        or      t_idmr,#cm0d                ; restart DMA compare 0 channel

}

        iret                                ; return from interrupt

;*****************************************************************************

;                     I/O port initialization

proc    INIT_IO [ PPR ]     {
;programmation  Port 5 in OUTPUT in DMA mode

        spp     #P5C_PG                     ; Port 5 control register page
                                            ; Port 5 in DMA mode
                                            ; Port 5 Handshake disabled
                                            ; DMA on Compare 0 channel

;                     76543210

        ld      P5C0R,#00000000b
        ld      P5C1R,#11111111b
        ld      P5C2R,#00000000b
        ld      P5DR,#0

        ld      HDC5R,#( hsdis | den | ddw | dcm0 )

;.......................end  init P5

}
```

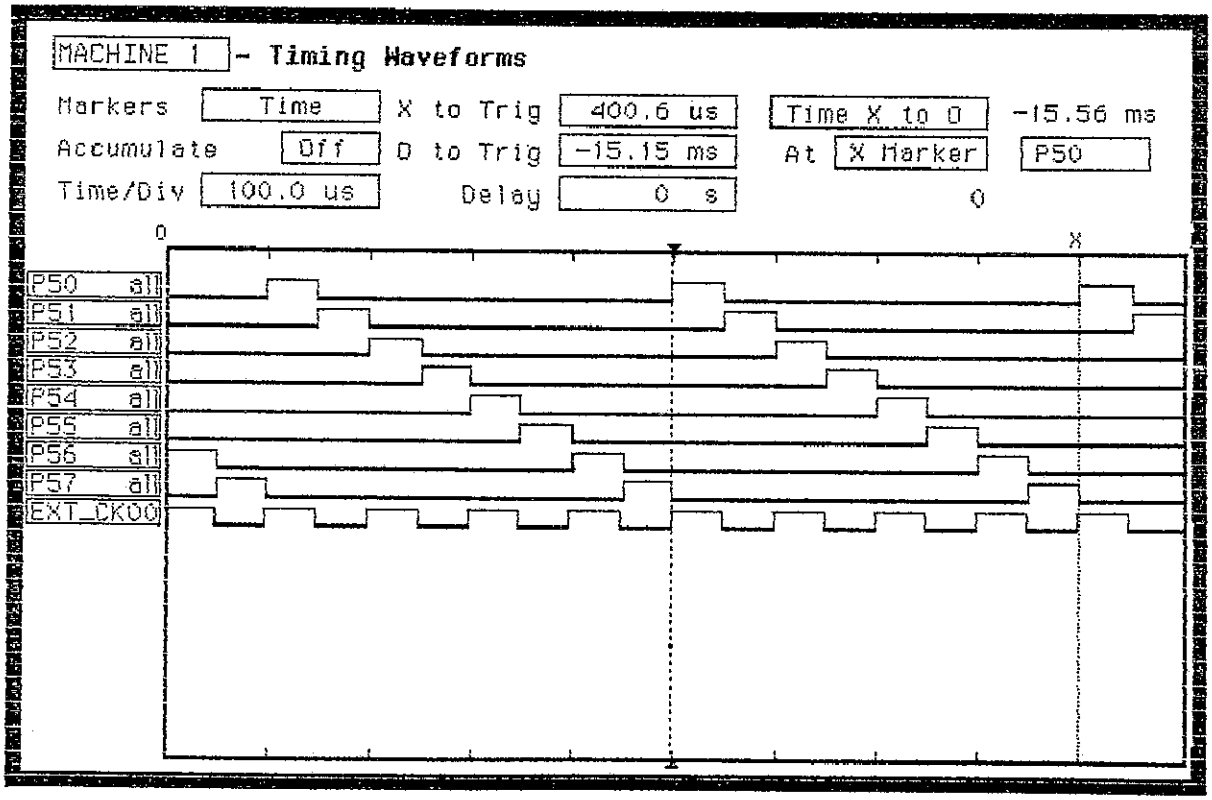
APPENDIX A: COMPARE 0 CHANNEL IN EXTERNAL MODE (Continued)

```
;*****************************************************************************
;               SECTION CODE FOR THE CORE INTERRUPT ROUTINE
;*****************************************************************************


;_____________________________________________  ;         INTERRUPT ROUTINE FOR ZERO DIVISION
;_____________________________________________

DIV0:   jx      DIV0                ; debug loop
        ret


;_____________________________________________  ;         INTERRUPT ROUTINE FOR TOP_LEVEL_IT
;_____________________________________________

TOP_LEVEL_IT:

        jx      TOP_LEVEL_IT        ; debug loop
        iret
```

APPENDIX B: CAPTURE 0 CHANNEL IN EXTERNAL MODE

The goal of the following example is to generate the following waveform synchronized by an external clock signal.

Figure 9. Timing Waveform Example: CAPTURE 0 Channel in External Mode



In this mode the Timer is programmed in CAPTURE 0 DMA external mode in order to output data located in program memory to I/O port 5. The data is output on Port 5 on each rising and falling edge of the external input clock (see the Timer initialization routine TIMER_1). A CAPTURE 0 interrupt (DMA end of block interrupt) resets the successful CAPTURE 0 flag and restarts the DMA transfer. I/O Port 5 is programmed in output in DMA mode and T1INA in input mode (see INIT_IO subroutine).

APPENDIX B: CAPTURE 0 CHANNEL IN EXTERNAL MODE (Continued)

```
.title  “DMA between program memory and I/O port 5 with timer 1 CAPTURE 0 channel”
;This program is a small example of using Timer 1 DMA external mode on I/O port
;The timer is programmed in CAPTURE0 DMA channel EXT mode
;***************************
;*INTERRUPT VECTOR ADDRESSES*
;***************************
CORE_IT_VECT          :=    00h             ; Core interrupts vectors
T1_IT_VECT            :=    10h             ; Timer 1 interruts vectors
CAPT_IT_VECT          =     4               ; CAPTURE event interrupt addres
COMP_IT_VECT          =     6               ; COMPARE event interrupt addres
T1_LEVEL              :=    4               ; Timer 1 priority level
LG_DMA                =     8               ; length of DMA
; Define the DMA pointer register
; DMA transfer from program memory
AD_DMA_BR             =     48h             ; DMA address base register
LG_DMA_BR             =     4ch             ; DMA counter base register
CPT_AD_DMA            :=    RR#AD_DMA_BR    ; Capture DMA address register pointer
CPT_LG_DMA            :=    RR#LG_DMA_BR    ; Capture DMA counter register pointer
; Define global references
.global         CAPTURE0, TIMER_1, INIT_IO, RESET_START, DMA_TABLE_OUT
;********************
;*Group number names*
;********************
BKC     :=      12
BKD     :=      13
BKE     :=      14
BKF     :=      15
BK_F    :=      BKF * 2                     ; group F: page registers
;***********************
;* Start Timer 1 macro *
;***********************
.macro  START_T1
        spp     #T1D_PG                     ; select Timer 0 page
        or      T_TCR,#( cen | ccl )        ; counter enable bit, clear counter
.endm
```

APPENDIX B: CAPTURE 0 CHANNEL IN EXTERNAL MODE (Continued)

```
;******************
;*START of PROGRAM*
;******************
;
START_PROG            :=    110h                    ; start address program

;********************
;*STACK Declaration*
;********************
;
SSTACK                :=    ( BKE * 16 ) - 1        ; System stack address group D C

USTACK                :=    ( BKC * 16 ) - 1        ; User stack address group B

;*****************************************
;*Declaration of the interrupt vectors table*
;*****************************************
;
                .text                               ; Start of program

                .org  CORE_IT_VECT                  ; Core interrupt vector
                                                    ; ********************

                .word RESET_START                   ; Power on interrupt vector

                .word DIV0                          ; Divided by 0 trap vector
                .word TOP_LEVEL_IT                  ; Top level interrupt vector
                .org  T1_IT_VECT                    ; Timer 1 interrupt vectors
                                                    ; ************************

                .org  T1_IT_VECT + CAPT_IT_VECT     ; Unused address

                .word CAPTURE0                      ; Timer 1 capture 0 interrupt

;******************************
;* Output data table to Port 5 *
;******************************
;
                .org  100h

DMA_TABLE_OUT:  .byte 01h, 02h, 04h, 08h

                .byte 10h, 20h, 40h, 80h            ; Output DMA table

;**********************
;*Start of main module*
;**********************
;
                .org  START_PROG                    ; Start of code

RESET_START:

        ld      MODER,#11100000b                    ; CLOCK MODE REGISTER
                                                    ; internal stack
                                                    ; no prescaling
                                                    ; external clock divided by 2

        ld      CICR,#10001111b                     ; CENTRAL INTERRUPT CONTROL REGISTER
                                                    ; priority level = 7
                                                    ; Nested Arbitration mode
                                                    ; disable interrupt
                                                    ; enable counters
                                                    ; At reset, Global Counter Enable
                                                    ; bit is active.

        ld      SSPLR,#SSTACK + 1                   ; load system stack pointer
        ld      USPLR,#USTACK + 1                   ; load user stack pointer
```

APPENDIX B: CAPTURE 0 CHANNEL IN EXTERNAL MODE (Continued)

```
        call    TIMER_1                             ; Timer 1 initialization  in DMA mode
        call    INIT_IO                             ; Port 5 init. DMA mode
        START_T1                                    ; Start Timer 1
        ei                                          ; enable all interrupts
;MAIN PROGRAMM
        loop    {
;               wfi
        }
;******************
;initialize TIMER 1
;******************
proc    TIMER_1 {
        srp     #BK_F                               ; select working register
        spp     #T1D_PG                             ; select timer 1 register page
        ld      t_tcr,#( ccp0 | udc )               ; count up
                                                    ; clear on capture 0
        ld      t_tmr,#rm0                          ; Disable output B
                                                    ; Disable output A
                                                    ; Internal clock
                                                    ; Countinuous mode
                                                    ; Capture on REG0
        ld      t_icr,#( ab_ti | exa_rf )           ; T1INA trigger, T1INB I/O
                                                    ; T1INA rising/falling edge sensitive
        clr     t_prsr                              ; No prescaling
        ld      t_oacr,#( ou_nop | c1_nop | c0_nop ); No action on OUTPUT0
        ld      t_obcr,#( ou_nop | c1_nop | c0_nop ); No action on COMPARE 0
                                                    ; on OUTPUT1
        clr     t_flagr
        spp     #T1C_PG                             ; Timer 1 Control page register
        ld      t1_dcpr,#LG_DMA_BR                  ; DMA counter register base address
        ld      t1_dapr,#AD_DMA_BR                  ; DMA address register base address
        ld      t1_ivr,#T1_IT_VECT
        ld      t1_idcr,#( T1_LEVEL | dcts )        ; DMA capture transaction source
        ldw     CPT_LG_DMA,#LG_DMA                  ; Capture DMA counter init.
        ldw     CPT_AD_DMA,#DMA_TABLE_OUT           ; Capture DMA addres init.
        spp     #T1D_PG                             ; Timer 1 Data page
        ld      t_idmr,#( gtien | cp0i | cp0d )     ; Capture 0 INT and DMA
}
```

APPENDIX B: CAPTURE 0 CHANNEL IN EXTERNAL MODE (Continued)

```
;*****************************************************************************
;                     CAPTURE 0 INTERRUPT ROUTINE
;                     DMA Interrupt End of block
;*****************************************************************************
;
CAPTURE0:

begin   [ PPR, RP0R, RP1R ] {               ; save page pointer
                                            ; save register pointer pair
        spp     #T1D_PG                     ; Timer 1 data register page
        srp     #BK_F                       ; select group F

        and     t_flagr,#~( cp0 | ocp0 )    ; reset successful capture 0
                                            ; reset overrun on capture 0

        ldw     CPT_LG_DMA,#LG_DMA

        ldw     CPT_AD_DMA,#DMA_TABLE_OUT

        or      t_idmr,#cp0d                ; restart DMA capture 0 channel

}

        iret                                ; return from interrupt

;*****************************************************************************
;                     I/O port initialization

proc    INIT_IO [ PPR ]     {

;programmation  Port 5 in OUTPUT in DMA mode

        spp     #P5C_PG                     ; Port 5 control register page
                                            ; Port 5 in DMA mode
                                            ; Port 5 Handshake disbled
                                            ; DMA on Capture 0 channel
                                            ; DMA direction = output

;                     76543210

        ld      P5C0R,#00000000b
        ld      P5C1R,#11111111b
        ld      P5C2R,#00000000b
        ld      P5DR,#0

        ld      HDC5R,#( hsdis | den | ddw | dcp0 )

;.......................  end init P5

; programmation P3.4 ( T1INA ) in INPUT, TRISTATE, TTL

        spp     #P3C_PG
        ld      P3C0R,#00010000b
        ld      P3C1R,#00000000b
        ld      P3C2R,#00010000b

}
```

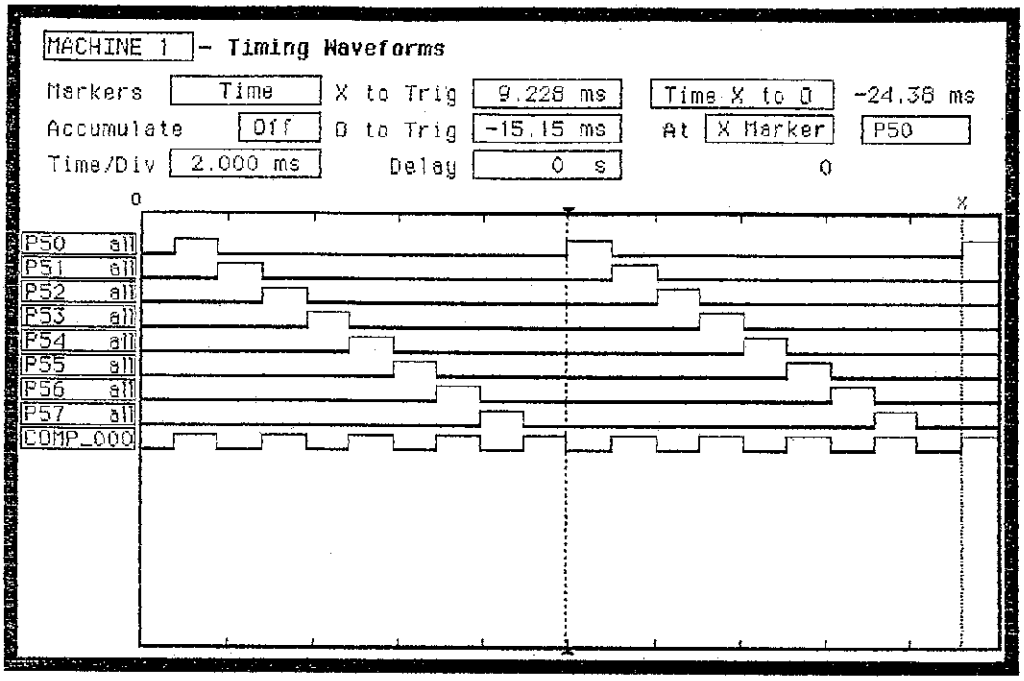
APPENDIX B: CAPTURE 0 CHANNEL IN EXTERNAL MODE (Continued)

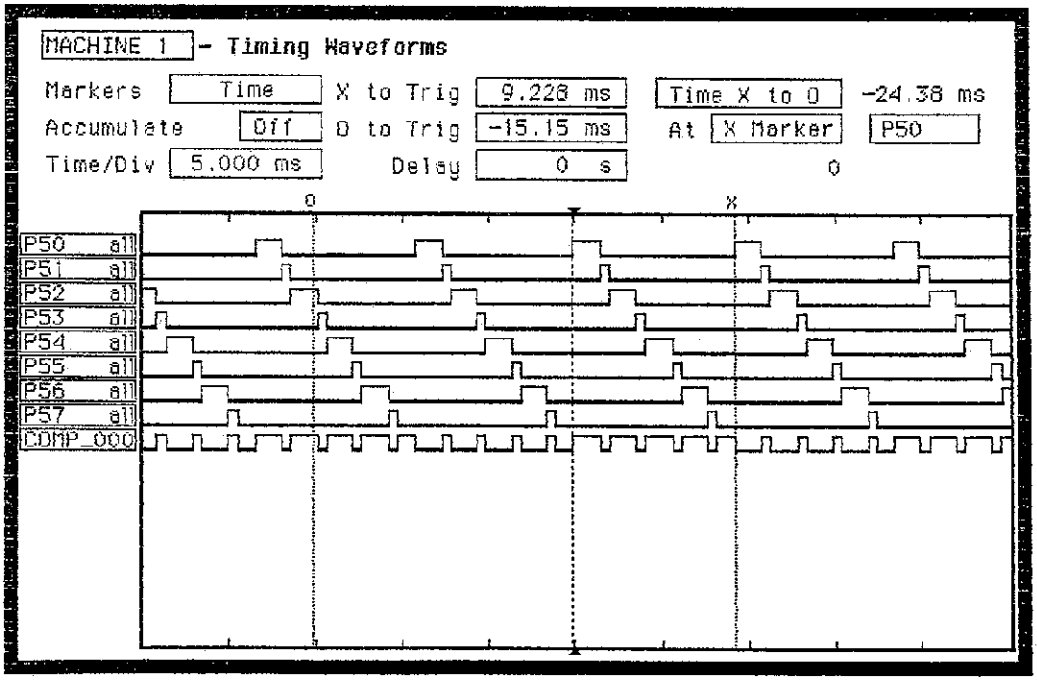
```
;*****************************************************************************
;               SECTION CODE FOR THE CORE INTERRUPT ROUTINE
;*****************************************************************************

;_____________________________________________
;               INTERRUPT ROUTINE FOR ZERO DIVISION
;_____________________________________________

DIV0:

        jx      DIV0                ; debug loop
        ret

;_____________________________________________
;               INTERRUPT ROUTINE FOR TOP_LEVEL_IT
;_____________________________________________

TOP_LEVEL_IT:

        jx      TOP_LEVEL_IT        ; debug loop

        iret
```

APPENDIX C: CAPTURE 0 CHANNEL SYNCHRONIZED BY COMPARE 0 CHANNEL

This example output data on the CAPTURE 0 channel in external mode is synchronized by a COMPARE 0 data transfer to provide the following waveform.

Figure 10. Timing Waveform Example: DMA Channel





APPENDIX C: CAPTURE 0 CHANNEL SYNCHRONIZED BY COMPARE 0 CHANNEL(Continued)

The DMA transfer uses two data tables located in program memory : DMA_TABLE_OUT, a list of data to be output on I/O Port 5 and DMA_TIME_TABLE, a list of the time value to be loaded in the COMPARE 0 register. In this mode the Timer is programmed on CAPTURE mode with DMA transfer on CAPTURE 0 and COMPARE 0 event. T1OUTA, toggled on each COMPARE 0 event, and T1INA are connected together in order to synchronize the data transfer on the I/O port (see TIMER_1 subroutine). A COMPARE 0 interrupt (end of DMA interrupt) resets the successful CAPTURE 0 and COMPARE 0 flag and restarts the two DMA transfers (see COMPARE 0 interrupt routine). I/O Port 5 is programmed in output in DMA mode, T1INA in input mode and T1OUTA in alternate function.

APPENDIX C: CAPTURE 0 CHANNEL SYNCHRONIZED BY COMPARE 0 CHANNEL(Continued)

```
.title  "DMA between program memory I/O port 5 with timer 1 DMA channel synchronization"

;This program is a small example of using Timer 1 DMA external mode on I/O port
;The timer is programmed in COMPARE 0 and CAPTURE 0 DMA mode with DMA channel
;Synchronization

;***************************
;*INTERRUPT VECTOR ADDRESSES*
;***************************

CORE_IT_VECT          :=    00h             ; Core interrupts vectors
T1_IT_VECT            :=    10h             ; Timer 1 interruts vectors

COMP_IT_VECT          =     6               ; COMPARE event interrupt addres
T1_LEVEL              =     4               ; Timer 1 priority level
LG_DMA                =     10              ; Length of DMA

; Define the DMA pointer register
; DMA transfer from program memory

AD_DMA_BR             =     48h             ; DMA address base register
LG_DMA_BR             =     4ch             ; DMA counter base register
CPT_AD_DMA            :=    RR#AD_DMA_BR    ; Capture DMA address register pointer
CPT_LG_DMA            :=    RR#LG_DMA_BR    ; Capture DMA counter register pointer
CMP_AD_DMA            :=    RR#AD_DMA_BR+2  ; Compare DMA address register pointer
CMP_LG_DMA            :=    RR#LG_DMA_BR+2  ; Compare DMA counter register pointer

; Define global references

.global         TIMER_1, INIT_IO, RESET_START, DMA_TABLE_OUT
.global         DMA_TIME_TABLE, COMPARE0

;********************
;*Group number names*
;********************

BKC                   :=    12
BKD                   :=    13
BKE                   :=    14
BKF                   :=    15
BK_F                  :=    BKF * 2         ; group F: page registers

;***********************
;* Start Timer 1 macro *
;***********************

.macro  START_T1

        spp     #T1D_PG                     ; select Timer 0 page
        or      T_TCR,#( cen | ccl )        ; counter enable bit, clear counter
.endm

;******************
;*START of PROGRAM*
;******************

START_PROG            :=    200h            ; start address program

;******************
;*STACK Declaration*
;******************

SSTACK                :=    ( BKE * 16 ) - 1; System stack address group D C
USTACK                :=    ( BKC * 16 ) - 1; User stack address group B
```

APPENDIX C: CAPTURE 0 CHANNEL SYNCHRONIZED BY COMPARE 0 CHANNEL(Continued)

```
;*****************************************
;*Declaration of the interrupt vectors table*
;*****************************************
;
        .text                                   ; start of program

                .org  CORE_IT_VECT              ; Core interrupt vector
                                                ; ********************
                .word RESET_START               ; power on interrupt vector
                .word DIV0                      ; divided by 0 interrupt vector
                .word TOP_LEVEL_IT              ; Top level interrupt vector

                .org  T1_IT_VECT                ; Timer 1 interrupt vectors
                                                ; ************************

                .org  T1_IT_VECT + COMP_IT_VECT ; unused addresses
                .word COMPARE0                  ; Timer 1 compare 0 interrupt

;*******************************
;* Output data table on Port 5 *
;*******************************
;
                .org  100h

DMA_TABLE_OUT:  .byte 00h, 01h, 02h, 04h, 08h
                .byte 10h, 20h, 40h, 80h, 00h           ; Output DMA table

;***********************************
;* Compare 0 channel DMA time table *
;***********************************
;
DMA_TIME_TABLE: .word 1000h, 2000h, 3000h, 4000h, 5000h
                .word 6000h, 7000h, 8000h, 9000h, 1000h ; Compare 0 Time Table

;**********************
;*Start of main module*
;**********************
;
                .org  START_PROG                ; Start of code
RESET_START:
        ld      MODER,#11100000b                ; CLOCK MODE REGISTER
                                                ; internal stack
                                                ; no prescaling
                                                ; external clock divided by 2

        ld      CICR,#10001111b                 ; CENTRAL INTERRUPT CONTROL REGISTER
                                                ; priority level = 7
                                                ; Nested Arbitration mode
                                                ; disable interrupt
                                                ; enable counters
                                                ; At reset, Global Counter Enable
                                                ; bit is active.

        ld      SSPLR,#SSTACK + 1               ; load system stack pointer
        ld      USPLR,#USTACK + 1               ; load user stack pointer

        call    INIT_IO                         ; Port 5 init. DMA mode

        call    TIMER_1                         ; Timer 1 initialization  in DMA mode

        START_T1                                ; Start Timer 1

        ei                                      ; enable all interrupts

;MAIN PROGRAMM
        loop    {
;               wfi
        }
; END OF MAIN PROGRAM
```

APPENDIX C: CAPTURE 0 CHANNEL SYNCHRONIZED BY COMPARE 0 CHANNEL(Continued)

```
;******************
;initialize TIMER 1
;******************
;
proc    TIMER_1 {

        srp     #BK_F                                   ; select working register
        spp     #T1D_PG                                 ; select timer 1 register page

        ld      t_tcr,#udc                              ; count up

        ld      t_tmr,#( oe0 | rm0 )                    ; Disable output B
                                                        ; Enable output A
                                                        ; Internal clock
                                                        ; Countinuous mode
                                                        ; Capture on REG0

        ld      t_icr,#( ab_ti | exa_rf )               ; T1INA trigger, T1INB I/O
                                                        ; T1INA rising and falling edge sensitive

        clr     t_prsr                                  ; No prescaling
        ld      t_oacr,#( ou_nop | c1_nop | c0_tog ); Toggle on Compare 0 event on T1OUTA
        ld      t_obcr,#( ou_nop | c1_nop | c0_nop ); No action on COMPARE 0 on T1OUTB

        clr     t_flagr

        spp     #T1C_PG                                 ; Timer 1 Control page register
        ld      t1_dcpr,#LG_DMA_BR                      ; DMA counter register base addres
        ld      t1_dapr,#AD_DMA_BR                      ; DMA address register base addres

        ld      t1_ivr,#T1_IT_VECT

        ld      t1_idcr,#( T1_LEVEL | dcts )            ; DMA capture transfer source
        ldw     CPT_LG_DMA,#LG_DMA                      ; Capture DMA counter init.
        ldw     CPT_AD_DMA,#DMA_TABLE_OUT               ; Capture DMA address init.
        ldw     CMP_LG_DMA,#( LG_DMA * 2 )              ; Compare DMA counter init.
        ldw     CMP_AD_DMA,#DMA_TIME_TABLE              ; Compare DMA address init.

        spp     #T1D_PG                                 ; Timer 1 Data page
        ldw     t_cmp0r,#0                              ; Clear Compare 0 register
        ld      t_idmr,#( gtien | cm0i | cm0d | cp0d ); DMA on Capture 0
                                                        ; Compare 0 INT and DMA

}
;*****************************************************************************
;                     COMPARE 0 INTERRUPT ROUTINE
;                     DMA Interrupt End of block
;*****************************************************************************
;
COMPARE0:

begin   [ PPR, RP0R, RP1R ] {                           ; save page pointer
                                                        ; save register pointer pair

        spp     #T1D_PG                                 ; Timer 1 data register page
        srp     #BK_F                                   ; select group F

        and     t_flagr,#~( cm0 | ocm0 | cp0 | ocp0 ); Reset successful Compare 0
                                                        ; Reset overrun on Compare 0
                                                        ; Reset successful Capture 0
                                                        ; Reset overrun on Capture 0
        or      t_tcr,#ccl                              ; Counter clear
```

APPENDIX C: CAPTURE 0 CHANNEL SYNCHRONIZED BY COMPARE 0 CHANNEL(Continued)

```
        ldw     CPT_LG_DMA,#LG_DMA-1
        ldw     CPT_AD_DMA,#DMA_TABLE_OUT+1
        ldw     CMP_LG_DMA,#( (LG_DMA-1) * 2 )
        ldw     CMP_AD_DMA,#DMA_TIME_TABLE+2
        or      t_idmr,#( cp0d | cm0d )             ; restart DMA capture 0 channel
                                                    ; restart DMA compare 0 channel

}

        iret                                        ; return from interrupt

;*****************************************************************************
;                    I/O port initialization

proc    INIT_IO [ PPR ]     {
;programmation  Port 5 in OUTPUT in DMA mode

        spp     #P5C_PG                             ; Port 5 control register page
                                                    ; Port 5 in DMA mode
                                                    ; Port 5 Handshake disbled
                                                    ; DMA on Capture 0 channel
                                                    ; DMA direction = output

;                       76543210

        ld      P5C0R,#00000000b

        ld      P5C1R,#11111111b

        ld      P5C2R,#00000000b

        ld      P5DR,#0

        ld      HDC5R,#( hsdis | den | ddw | dcp0 )

;.......................end  init P5

; programmation P3.4 ( T1INA ) in INPUT, TRISTATE, TTL
; programmation P3.5 ( T1OUTA ) in ALTERNATE FUNCTION, PUSH-PULL, TTL

        spp     #P3C_PG
        ld      P3C0R,#00110000b
        ld      P3C1R,#00100000b
        ld      P3C2R,#00010000b

}
;*****************************************************************************
;               SECTION CODE FOR THE CORE INTERRUPT ROUTINE
;*****************************************************************************

;_____________________________________
;               INTERRUPT ROUTINE FOR ZERO DIVISION
;_____________________________________

DIV0:

        jx      DIV0                                ; debug loop

        ret

;_____________________________________
;               INTERRUPT ROUTINE FOR TOP_LEVEL_IT
;_____________________________________

TOP_LEVEL_IT:

        jx      TOP_LEVEL_IT                        ; debug loop
        iret
```

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